

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: 09162301 A

(43) Date of publication of application: 20.06.1997

(51) Int. Cl. H01L 21/8238

H01L 27/092, H01L 29/78, H01L 21/336

(21) Application number: 07316329

(22) Date of filing: 05.12.1995

(71) Applicant: NEC CORP

(72) Inventor: UCHIDA TETSUYA

(54) SEMICONDUCTOR DEVICE AND
MANUFACTURE THEREOF

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device which comprises an insulated-gate field-effect transistor having a suppressed short-channel effect, shortened delay time and small variation of a threshold value, and a manufacturing method of the semiconductor device.

SOLUTION: In an insulated-gate field-effect transistor, first-conductivity type regions 15 and 16 for preventing expansion of the depletion layer are provided at a level a predetermined distance below the surface of the substrate 11. The first-conductivity regions 15 and 16 have a density higher than that of the substrate 11. Source diffusion layers 24 and 28 of a second-conductivity type are formed on the surface of the substrate 11, with their bottom surfaces positioned around peak density positions of the first-conductivity type regions 15 and 16 or closer to the surface of the substrate 11. Drain diffusion layers 25 and 29 of the second-conductivity

type are formed on the surface of the substrate 11, with their bottom surfaces positioned lower than the peak density positions of the first-conductivity type regions 15 and 16. Thus, the short channel effect can be suppressed, and the junction capacitance of drain diffusion layers can be reduced.

COPYRIGHT: (C)1997,JPO

